FLIP CHIP INTERCONNECTION STRUCTURE

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority from U.S. Provisional Application No. 60/188,570, titled "Flip Chip Interconnection Structure". This application is related to commonly assigned copending U.S. Application Atty. Docket No. 60084-300201 titled "Packaging Structure and Method" and U.S. Application Atty. Docket No. 60084-300101 titled "Flip Chip-in-Leadframe Package and Method"; both said related applications are being filed on the same date as this application, and are hereby incorporated by reference in their entireties herein.

BACKGROUND OF THE INVENTION

[0002] This invention relates to flip chip interconnection structures and, more particularly, to an interconnect structure formed by mechanical deformation and interlocking of asperities between the surfaces to be joined.

[0003] Flip chip interconnection between an integrated circuit (IC) chip and a substrate is commonly performed in electronic package assembly. In the most common form of such interconnection bumps on the IC chip are metallurgically joined to pads formed on the substrate, usually by melting of the bump material. While this approach provides robust connections, it is difficult to reduce the pitch of the interconnection due to the risk of bridging (i.e. shorting between adjacent connections) during the melting and solidification processes. In an alternative approach the attachment is made using a particulate film or paste, whereby conductive particles in the paste or film together with the shrinkage force of a resin effect an electrical connection. This approach lends itself to reduction of interconnection pitch but suffers from limited long term reliability owing to the susceptibility of the particulate interconnection to degrade over time.

BRIEF SUMMARY OF THE INVENTION

[0004] In one general aspect the invention features a method for forming a flip chip interconnection structure, by providing a first member on an IC chip and a second member on a substrate, in which the first member includes a deformable material having a low yield strength and a high elongation to failure and the second member has surface asperities on the part to be bonded with the first member; and pressing the first and second members against one another using a force sufficient to cause plastic flow of part of the first member into asperities on the second member.

[0005] In some embodiments the first member is a bump formed on the IC chip, and typically is one of a set of such bumps; and the deformable materials of the first member in some particularly useful embodiments includes gold. In some embodiments the second member is a lead or pad on the substrate, or is a via opening. In some embodiments the second member is a surface pad having a conventional plated surface finish, on which the asperities are provided according to the invention.

[0006] In another general aspect the invention features a flip chip interconnection structure made by the method of the invention.

[0007] In another general aspect the invention features a flip chip interconnection structure, which includes a first member attached to a chip and a second member attached to a substrate, in which the first member is of a deformable material and the first and second members are bonded by mechanical interlocking of the deformable material of the first member with asperities on the surface of the second member.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figs. 1A, 1B are diagrammatic sketches in a sectional view showing an illustrative embodiment according to the invention of steps in the formation of an assembly having a chip interconnection structure according to the invention.

[0009] Figs. 2A, 2B are diagrammatic sketches in a sectional view showing a second illustrative embodiment according to the invention of steps in the formation of an assembly having a chip interconnection structure according to the invention.

[0010] Figs. 3A, 3B are diagrammatic sketches in a sectional view showing a third illustrative embodiment according to the invention of steps in the formation of an assembly having a chip interconnection structure according to the invention.

[0011] Figs. 4A, 4B are diagrammatic sketches in a sectional view showing a fourth illustrative embodiment according to the invention steps in the formation of an assembly having a chip interconnection structure according to the invention.

[0012] Fig. 5 is a diagrammatic sketch in a sectional view showing an alternative shape for an interconnection bump useful according to the invention.

[0013] Fig. 6 is a diagrammatic sketch in a sectional view showing another alternative shape for an interconnection bump useful according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0014] With reference to Figs. 1A, 1B a flip chip interconnection structure generally designated 10 is shown schematically including a first member 12 and a second member 14. The first member 12 is preferably a bump formed on the IC chip and the second member 14 is preferably a lead or pad formed on the substrate. The first member 12 further preferably comprises a soft, deformable material with a low yield strength and high elongation to failure. The second member 14 further preferably includes a substrate pad with a conventional plated surface finish, and is characterized by having asperities 16, which are shown exaggerated in the Figs. for purposes of illustration. The scale of the asperities is generally in the order about 1 μm - 25 μm. The bump is a generally compliant material, that is to say, a material that, in the particular bump as shaped, undergoes a plastic deformation greater than about 25 μm under a force equivalent to a vertical load of about 250 grams. Gold can be a particularly useful material for the bumps according to the invention.

[0015] The interconnection is accomplished by compressing the first member 12 and the second member 14 against one another to cause plastic flow of first member 12 into asperities 16. The height and soft nature of first member 12 allows considerable deformation to occur even after the connection is effected thus allowing for other bump/pad pairs with poor planarity to be joined with equal success. The force and

temperature requirements necessary to effect the interconnection are significantly lower than needed for conventional thermo-compression bonds that require metallurgical diffusion of the mating materials. These reduced requirements greatly reduce damage that might otherwise occur on the chip, particularly when the number of connections to be effected simultaneously is large.

[0016] A second embodiment is schematically shown in Figs. 2A, 2B. A macroscopic interlocking configuration generally designated 20 is formed by plastic flow of the material of first member 22 around a side wall 24 and edge 26 of a second member or trace 28. Preferably the flow of the material of first member 22 is around the side wall 24 and does not cause material flow into a region between adjacent traces but rather in the normal direction within the same plane. The interlocking configuration 20 provides for an increased area of interlocked surfaces without significantly increasing the bonding force, thereby providing a more robust connection. Further the additional displacement perpendicular to the chip surface provides greater tolerance to poor co-planarity of multiple mating surface. Finally, the interlocking along a plane perpendicular to the chip surface in addition to the usual interlocking parallel to the chip surface provides for protection against relative movement between the die and the substrate in a perpendicular direction.

[0017] A third embodiment is shown in Figs. 3A, 3B and includes an interconnection generally designated 30. The interconnection 30 is formed by plastic flow of the material of a first member 32 around a second member 34. The second member 34 includes a smaller width than that of the first member 32 which allows for plastic flow of the material of first member 32 around both sides 36 and 38 of the second member 34.

[0018] A fourth embodiment is shown in Figs. 4A, 4B and includes an interconnection generally designated 40. The lead geometry of a second element 42 is shown to be wedge shaped to take advantage of what represents the most typical "undercut" lead shape in actual substrates that are fabricated by the subtractive etching method. The interconnection 40 is formed by plastic flow of the material of a first element 44 around the second element 42. The shown geometry removes the restriction of minimum trace width and more specifically the minimum width of a plateau 46 necessary for conventional wire bonding applications. It is contemplated that the

interconnection 40 could alternatively be formed by bonding directly on a via pad or through a via hole down to the next lower layer on the substrate.

[0019] In embodiments as described above with reference to Figs. 2A, 2B, 3A, 3B, 4A, 4B, the macroscopic interlocking configuration allows for formation of the interconnect using a lower force, for example lower by a factor of 2, as compared with embodiments as described above with reference to Figs. 1A, 1B. Use of lower force of compression can result in less damage to chips during processing.

[0020] In preferred embodiments, an adhesive resin is preferably applied in a space between the chip and the substrate such that the compressive force supplied by the cured resin further improves the long-term retention of the electrical connection. The adhesive resin is preferably applied before the mating surfaces are bonded, and is cured concomitantly with the formation of the interconnection. The applied interconnection force helps displace the resin material away from the mating surfaces to allow the formation of the desired mechanically interlocked connection. Alternatively, the resin can be applied after the interconnection using an underfill process.

[0021] In the disclosed preferred embodiments, the material of the first members 12, 22, 32 and 44 is preferably Cu, electroless NiAu or Au. The substrate material is preferably single-sided FR5 laminate or 2-sided BT-resin laminate.

[0022] The bumps may have various configurations other than one shown in the Figs. above having a generally rectangular section before compression and deformation; two particularly useful ones are shown diagrammatically in Figs. 5 and 6. Fig. 5 shows a "stepped" shape, in which the portion of the bump adjacent the chip (the "base") is wider than the portion (the "tip") that will be compressed against the pad on the substrate. Fig 6 shows a "stud bump" configuration, in which the base has a peripherally rounded profile that is wider than the tip. Either of these constructs can provide improved compliance of the bump with the asperities on the substrate, owing to the thinner tip dimension, and also provide good structural stability owing to the wider profile of the base.

[0023] The second member may be a lead or a pad, as described above, and a bump may be interconnected to a conventional solder pad that is electrically connect to

a via hole; but in some embodiments the second member itself includes a via hole. According to this embodiment of the invention an interconnection structure can be formed directly between the bump and the via hole, by compressing the bump directly against conductive material in and at the margin of the via hole, rather than compressing the bump onto a pad, such as a solder pad, formed at some distance away from the via hole and connected to it. This results in a more efficient use of the area on the chip. Where the opening in the via hole is generally smaller than the tip of the bump, then the bump can be pressed directly onto the via hole, and becomes deformed into the via hole to form the interconnection; in effect, the via hole works as the asperity in this construct. where the bump is smaller than the via hole, then the bump can be offset, so that the bond is formed at a portion of the rim of the via opening.